Se dispone de un sistema multiprocesador con 4 procesadores. Para mantener la coherencia entre la memoria principal y las cachés de los procesadores, se utiliza un protocolo de invalidación MESI. A partir del siguiente estado inicial, indica como evolucionaría el estado de las cachés y la memoria principal para las siguientes referencias a memoria:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | C1 | | | C2 | | | C3 | | | C4 | | |  | MP | | | |
|  | @1 | 5 | M | @2 | 5 | S | @1 | 10 | I | @3 | 1 | I |  | @1 | 10 | @3 | 0 |
|  | @3 | 1 | I | @3 | 0 | S | @2 | 5 | S | @4 | 2 | M |  | @2 | 5 | @4 | 1 |

* Rd1(@4)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | C1 | | | C2 | | | C3 | | | C4 | | |  | MP | | | |
|  | @1 | 5 | M | @2 | 5 | S | @1 | 10 | I | @3 | 1 | I |  | @1 | 10 | @3 | 0 |
|  | @4 | 2 | S | @3 | 0 | S | @2 | 5 | S | @4 | 2 | S |  | @2 | 5 | @4 | 2 |

La dirección @4 se encuentra modificada en C4, así que se interceptará la señal de lectura para realizar un flush del dato. En C1 será sustituido por @3 al ser este dato invalido, si no hubiera ningún dato invalido tomaríamos un protocolo de sustitución aleatoria ya que no se especifica nada en el enunciado.

* Wr4(@2,10)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | C1 | | | C2 | | | C3 | | | C4 | | |  | MP | | | |
|  | @1 | 5 | M | @2 | 5 | I | @1 | 10 | I | @2 | 10 | M |  | @1 | 10 | @3 | 0 |
|  | @4 | 2 | S | @3 | 0 | S | @2 | 5 | I | @4 | 2 | S |  | @2 | 5 | @4 | 2 |

Sustituimos la dirección @3 por @2 con el dato a escribir y lo ponemos a modificado. En C2 y C3 cambiamos @2 a inválido.

* Rd3(@2)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | C1 | | | C2 | | | C3 | | | C4 | | |  | MP | | | |
|  | @1 | 5 | M | @2 | 5 | I | @1 | 10 | I | @2 | 10 | S |  | @1 | 10 | @3 | 0 |
|  | @4 | 2 | S | @3 | 0 | S | @2 | 10 | S | @4 | 2 | S |  | @2 | 10 | @4 | 2 |

C4 hace un flush de @2 y C3 sustituye un invalido por el valor 10. Ambos se ponen a compartido.

* Rd1(@1)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | C1 | | | C2 | | | C3 | | | C4 | | |  | MP | | | |
|  | @1 | 5 | M | @2 | 5 | I | @1 | 10 | I | @2 | 10 | S |  | @1 | 10 | @3 | 0 |
|  | @4 | 2 | S | @3 | 0 | S | @2 | 10 | S | @4 | 2 | S |  | @2 | 10 | @4 | 2 |

Acierto de lectura, nada cambia.